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EXAMINER	
LEE, CHRISTOPHER E	
ART UNIT	**PAPER NUMBER**
2112	

DATE MAILED: 08/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/052,277	JENSEN, JENSEN HARTRUNG	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-13 and 15-19* is/are rejected.

7)☒ Claim(s) *8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 15th of April 2005. Claims 1, 8, 10 and 18 have been amended; claim 14 has been canceled; and no claim has been newly added since the Non-Final Office Action was mailed on 22nd of June 2004. Currently, claims 1-13 and 15-19 are pending in this Application.

Examiner's Notice

2. The Amendment document in the Response is considered non-compliant because it has failed to meet the requirements of 37 CFR 1.121, as amended on June 30, 2003 (*See 68 Fed. Reg. 38611*, Jun. 30, 2003). In fact, the claim status of the claims 2-7, 9, 11-13, 15, 16, and 19 are not (Previously presented), but (Original). Further, the claim 17 does not have any status of the claim, which is required by 37 CFR 1.121, as amended on June 30, 2003. See MPEP 714 [R-2] and 37 CFR 1.121(c).

Specification

3. The disclosure is objected to because of the following informalities:

Substitute "the interface 320" by --the interface 125-- on page 6.

Appropriate correction is required.

4. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: the specification fails to provide the claimed limitation "the bus controller includes one or more devices that operate in dependence up the enabling signal" in lines 2-3 of the claim 8 under a proper antecedent basis.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. However, the limitation "the bus controller includes one or more

devices that operate in dependence up to the enabling signal" in lines 2-3 of the claim 8 is not shown in the drawings. Therefore, the limitation must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 9 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

In the specification, paragraph [0016], the application discloses that an initiator of the plurality of initiators is configured to provide a pre-notification signal, which is different from the initiation signal of a data-transfer operation, to the activity detector before it communicates command or data information to the bus. However, the claim 9 recites that a component (i.e., initiator) of the plurality of components (i.e., initiators) is configured to signal the initiation of the data-transfer operation, which is not the pre-notification signal, to the activity detector before the component (i.e., initiator) initiates the data-transfer operation via the bus structure.

The Examiner doubts how the component is configured to signal the initiation of the data-transfer operation before the component actually initiates the data-transfer operation via the bus structure. In other words, the component should initiate the data-transfer operation in order to signal the initiation of the data-transfer operation via the bus structure to the activity detector.

Therefore, the claim 9 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention.

For the purpose of claim rejection, the Examiner presumes "...is configured to signal **for** the initiation of the data-transfer operation to ..." in line 2 since it fails to comply with 35 U.S.C. §112, first paragraph, scope enablement requirement.

8. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 11 and 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Each of the claims 11 and 13 recites the limitation "the one or more other components" in lines 2-3 of the claim 11, and in line 3 of the claim 13, respectively. There is insufficient antecedent basis for this limitation in the claim. Therefore, the Examiner presumes the term "the one or more other components"

could be considered as --the more than one other components-- since it is not clearly defined in the claims.

Claim Rejections - 35 USC § 102

10. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

11. Claims 1-7, 9-13 and 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Mitchell et al. [US 5,987,614 A; hereinafter Mitchell].

Referring to claim 1, Mitchell discloses a system (i.e., distributed power management system; See col. 1, lines 5-10) comprising:

- a plurality of components (i.e., CPU 40, Subsystem 1, ... Subsystem n in Fig. 3) each having a bus interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3),
- a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3) that is configured to facilitate communications among said plurality of components (See col. 7, lines 39-54), and
- an activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) that is configured to detect an initiation of a data-transfer operation (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular bus cycle) and to provide therefrom an enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) that is communicated to bus interfaces (i.e., said core logics for Subsystems in Fig. 3) of a plurality of said components (i.e., CPU, Subsystem 1, ... Subsystem n), wherein
    - said bus interface (i.e., said core logic) is configured to be enabled to receive data from said bus structure upon receipt of said enabling signal from said activity detector (See col. 7, line 59 through col. 8, line 3).

Referring to claim 2, Mitchell teaches

- said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) is configured to detect a completion of said data-transfer operation (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and terminates said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) based on said completion of said data-transfer operation (See col. 8, lines 5-6), and
- said bus interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) is configured to be disabled from receiving data from said bus structure upon termination of said enabling signal (See col. 8, lines 6-8).

Referring to claim 3, Mitchell teaches

- said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) includes a gated clock signal (i.e., gbclk 67 from control gate logic 63 in Fig. 7).

Referring to claim 4, Mitchell teaches

- said bus interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) includes a plurality of clocked devices (i.e., And gates 521 and 522 in Fig. 6) that are clocked based on said enabling signal (i.e., being clocked by gbclk in Fig. 6).

Referring to claim 5, Mitchell teaches said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) includes:

- a set-reset device (i.e., Flip-Flop 106 of Fig. 7) that is set (i.e., en^+ appearance from Flip-Flop 106 in Fig. 7) upon detection of said initiation of said data-transfer operation (See col. 7, lines 55-57 and col. 13, lines 47-58), and

- a delay device (i.e., Flip-Flop 107 of Fig. 7), operably coupled to said set-reset device (See col. 14, lines 7-12), that is configured to provide said enabling signal (i.e., gbclk 67 of Fig. 7) synchronous with a system clock (i.e., gbclk is synchronized with bus clock bclk in Fig. 8) that is common to said bus structure (i.e., bus system clock; See col. 7, lines 38-43), based on whether said set-reset device is set (See col. 13, lines 56-60).

Referring to claim 6, Mitchell teaches

- said set-reset device (i.e., Flip-Flop 106 of Fig. 7) is reset (i.e., en^+ disappearance from Flip-Flop 106 in Fig. 7) upon detection of a completion of said data-transfer operation (See col. 8, lines 3-8 and col. 13, lines 58-60).

Referring to claim 7, Mitchell teaches

- a bus controller (i.e., Address Decode Logic 91 and Address Comparison Logic 92 in Fig. 4) that is configured to establish a communications path (See col. 18, lines 3-25 and Fig 16) between an initiating component (i.e., CPU 40 or any Subsystem requesting resources on a target Subsystem in Fig. 3) of said plurality of components (i.e., CPU 40, Subsystem 1, ... Subsystem n in Fig. 3) and a target component (e.g., Subsystem 1 51 in Fig. 3) of said plurality of components,
    - wherein said activity detector (i.e., said Address Comparison Logic and Clock Control Gate Logic) provides said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) within a time duration consumed by said bus controller to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for providing the enabling signal because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates said activity detector providing

said enabling signal within a time duration consumed by said bus controller to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

Referring to claim 9, Mitchell teaches

- a component of said plurality of components (e.g., CPU 40 in Fig. 3) is configured to signal (i.e., sending subsystem address; See col. 6, lines 7-8) for said initiation of said data-transfer operation (i.e., for starting a communication) to said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4; See col. 6, lines 9-18) before said component (i.e., CPU) initiates said data-transfer operation via said bus structure (in fact, said subsystem address sent by CPU should be identified by Address Decode Logic 91 and Address Comparison Logic 92 in Fig. 4 before the communication is activated; See col. 6, lines 7-18).

Referring to claim 10, Mitchell discloses a method of reducing power consumption in a system (i.e., distributed power management system; See col. 3, lines 66-67) comprising

- a plurality of components (i.e., CPU 40, Subsystem 1, ... Subsystem n in Fig. 3) each having a bus interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3), that are configured to communicate via a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3; See col. 7, lines 39-54), comprising:
    - detecting an initiation of bus activity (i.e., accessing resources via a bus) by a component of said plurality of components (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular bus cycle requiring resources within a subsystem of the plurality of components by one of the plurality of components, e.g., CPU),

- communicating an enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) to more than one other components of said plurality of components (e.g., Subsystem 1 51 and Subsystem n in Fig. 3), and
- enabling a bus interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) at each of said more than one other components (i.e., said Subsystem 1 and Subsystem n) to receive signals corresponding to said bus activity, based on said enabling signal (See col. 7, line 59 through col. 8, line 3).

Referring to claim 11, Mitchell teaches

- detecting a completion of said bus activity (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and
- disabling said bus interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) at each of said more than one other components (i.e., Subsystem 1 51 and Subsystem n in Fig. 3), based on said completion of said bus activity (See col. 8, lines 5-8).

Referring to claim 12, Mitchell teaches

- synchronizing (i.e., gbclk is synchronized with bus clock bclk in Fig. 8) said enabling signal (i.e., gbclk 67 of Fig. 7) to a system clock (i.e., bclk 74 of Fig. 7) that is common to said bus structure (i.e., bus system clock being common to Bus clock 74 in Fig. 3; See col. 7, lines 38-43).

Referring to claim 13, Mitchell teaches

- establishing a communications path (See col. 18, lines 3-25 and Fig 16) between said component that initiated said bus activity (i.e., CPU 40 or any Subsystem requesting resources on a target

Subsystem in Fig. 3) and a target component (e.g., Subsystem 1 51 in Fig. 3) of said more than one other components (i.e., Subsystem 1 51 and Subsystem n in Fig. 3), and

- enabling said bus interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) at said target component within a time duration required to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for enabling said bus interface because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates the step of enabling said bus interface at said target component within a time duration required to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

Referring to claim 15, Mitchell discloses an electronic circuit (i.e., distributed power management system; See col. 1, lines 5-10) comprising:

- a plurality of initiators (i.e., Subsystem 1, ... Subsystem n in Fig. 3) that are configured to selectively initiate data-transfer operations (i.e., requesting resources which are included in target; See col. 7, lines 47-54) via a bus structure (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3),
- a plurality of targets (i.e., Subsystem 1, ... Subsystem n in Fig. 3) that are configured to process said data-transfer operations (i.e., providing requested resources; See col. 7, lines 55-61), each of said plurality of targets (e.g., Subsystem 1 51 in Fig. 3) including
    - an interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) for receiving said data-transfer operations, and
    - an activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) that is configured to detect an initiation of a data-transfer operation from any of said plurality of initiators (See col. 7, lines 43-46 and 55-57; i.e., detecting a particular

bus cycle), and to generate therefrom an enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3),

- wherein said interface (i.e., said core logic) of each of said plurality of targets is configured to receive said data-transfer operations in dependence upon said enabling signal from said activity detector (See col. 7, line 59 through col. 8, line 3).

Referring to claim 16, Mitchell teaches

- said plurality of initiators (i.e., Subsystem 1, ... Subsystem n in Fig. 3) are configured to effect said data-transfer operations at a system clock speed (i.e., bus clock bclk in Fig. 8; in fact, all the Subsystems are operating under the system bus clock bclk 74 in Fig. 3), and
- said interface (i.e., core logic 52, e.g., core logic 1 52a, in Fig. 3) of each of said plurality of targets is configured to operate at said system clock speed (i.e., bclk speed in Fig. 8) only when said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) provides said enabling signal (i.e., gbclk 57 in Fig. 3; See col. 13, line 40 through col. 14, line 13).

Referring to claim 17, Mitchell teaches said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) includes

- a clocking signal that operates at said system clock speed (i.e., a gated clock signal gbclk 67 from control gate logic 63 in Fig. 7).

Referring to claim 18, Mitchell teaches said activity detector is configured

- to detect a completion of said data-transfer operations (See col. 8, lines 3-5; i.e., detecting a completion of the particular bus cycle), and
- to terminate said generation of said enabling signal (e.g., disabling gbclk 57a of Fig. 3) based on a completion of said data-transfer operations (See col. 8, lines 5-8).

Referring to claim 19, Mitchell teaches

- a bus controller (i.e., Address Decode Logic 91 and Address Comparison Logic 92 in Fig. 4) that is configured to establish a communications path (See col. 18, lines 3-25 and Fig 16) between an initiator of said plurality of initiators (i.e., any one of Subsystems requesting resources on a target Subsystem in Fig. 3) and a target (e.g., Subsystem 1 51 in Fig. 3) of said plurality of targets,
    - wherein said activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) is configured to generate said enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) within a time duration required by said bus controller to establish said communications path (i.e., the time duration for establishing communication path from CPU to Subsystem 1 is longer than the time duration for providing the enabling signal because the communication path should be established after the activity detector generates the enabling signal, which clearly anticipates said activity detector is configured to generate said enabling signal within a time duration required by said bus controller to establish said communications path; See col. 7, line 38 through col. 8, line 3 and Fig. 3).

Allowable Subject Matter

12. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. The following is a statement of reasons for the indication of allowable subject matter:

With respect to claim 8, the claim limitations are deemed allowable over the prior art of record as the prior art fails to teach or suggest that said bus controller operates in dependence upon said enabling signal being provided by said activity detector.

Response to Arguments

14. The Examiner notes that there is a typographical error in the Response page 7, line 2, i.e., the date of the Office Action should be 22nd of June 2004 (described on page 1 of the Response) instead of September 15, 2004.

15. Applicant's arguments filed on 15th of April 2005 have been fully considered but they are not persuasive.

In response to the Applicant's argument with respect to "Claim 9 was rejected as being inadequately supported by the present specification. The rejection is respectfully. Support for claim 9 is believed to be found in the specification as originally filed, in paragraph 0016 and elsewhere." in the Response page 7, lines 8-10, the Examiner respectfully disagrees.

In the specification, paragraph [0016], the application discloses that an initiator of the plurality of initiators is configured to provide a pre-notification signal, which is different from the initiation signal of a data-transfer operation, to the activity detector before it communicates command or data information to the bus. However, the claim 9 recites that a component (i.e., initiator) of the plurality of components (i.e., initiators) is configured to signal the initiation of the data-transfer operation (i.e., informing (signaling) the initiation of actual data-transfer operation), which is not the pre-notification signal, to the activity detector before the component (i.e., initiator) actually initiates the data-transfer operation via the bus structure. Therefore, the claim 9 contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains to make and/or use the invention, and it fails to comply with 35 U.S.C. §112, first paragraph, scope enablement requirement. (See paragraph 7 of

the instant Office Action, Claim 9 rejection under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement).

Thus, the Applicant's argument on this point is not persuasive.

In response to the Applicant's reconsideration request with respect to "Claims 1-7, 10-13 and 15-19 were rejected as being anticipated by Mitchell. ... The independent claims have been amended to more clearly distinguish over the cited reference. ... In particular, the claims have been amended to recite an activity detector is configured to detect an initiation of a data-transfer operation on a common bus and to provide therefrom an enabling signal that is communicated to bus interfaces of a plurality of components coupled to the common bus through respective bus interfaces. Mitchell is not believed to teach or suggest such a feature. Rather, Mitchell teaches a single component coupled to a bus, the component being partitioned into a first portion that serves as an 'activity detector' for that component only." in the Response page 7, lines 11-20, the Examiner respectfully disagrees.

In contrary to the Applicant's assertion, i.e., Mitchell teaches a single component coupled to a bus, the component being partitioned into a first portion that serves as an 'activity detector' for that component only, Mitchell teaches a plurality of components (i.e., CPU 40, Subsystem 1, ... Subsystem n in Fig. 3) coupled to a bus (i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43 in Fig. 3), each component (e.g., Subsystem 1 of Fig. 3) having an activity detector (i.e., Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4) to provide therefrom an enabling signal (i.e., gbclk 57, e.g., gbclk 57a and gbclk 57n, in Fig. 3) that is communicated to bus interfaces (i.e., said core logics for Subsystems in Fig. 3) of a plurality of said components (i.e., CPU, Subsystem 1, ... Subsystem n). Refer to the paragraph 11 of the instant Office Action, claims 1-7, 9-13 and 15-19 rejection under 35 U.S.C. 102(b) as being anticipated by Mitchell.

Therefore, Mitchell clearly teaches the claimed limitations, such as Address Comparison Logic 92 and Clock Control Gate Logic 53 in Fig. 4 (i.e., activity detector) is configured to detect detecting a particular

bus cycle (i.e., detecting an initiation of a data-transfer operation; See Mitchell, col. 7, lines 43-46 and 55-57) on a common bus, i.e., Data 71, Address 72, Bus controls & status 73, Bus clock 74, Power down 75 and Central bus interface 43, and to provide therefrom gbclk 57, e.g., gbclk 57a and gbclk 57n, (i.e., enabling signal) that is communicated to core logics 52 (i.e., bus interfaces) of CPU 40, Subsystem 1, ... Subsystem n in Fig. 3 (i.e., a plurality of components) coupled to the common bus through respective core logics (i.e., bus interfaces; in fact, CPU and Subsystems are coupled to the common bus through respective core logics through Data line between the common bus and Core Logics in Fig. 3). Furthermore, the Applicant alleges that Mitchell teaches the component being partitioned into a first portion that serves as an 'activity detector' for that component only. However, it is noted that the features upon which applicant rely (i.e., a single activity detector for the plurality of components) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Thus, the Applicant's argument on this point is not persuasive.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bertin et al, [US 6,097,241 A] disclose ASIC low power activity detector to change threshold voltage.

17. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/ CEL

REHANA PERVEEN
PRIMARY EXAMINER
8/2/05